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Simulation Modeling and Performance Investigation of Cross switched T-type Multilevel Inverter

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***Abstract* — This paper presents and evaluates the performance of Cross Switched T-type (CT-type) MLI, which uses fewer (Eight) power electronic switches. The cross switched configuration is implemented by connecting two T-type modules back-to-back with the help of cross-connected switches. The novel configuration can be developed for both symmetrical and unsymmetrical voltage ratings. The model can be expanded to obtain higher voltage levels by cascading to the simple T-type configuration. The major contribution of this novel configuration is that negative voltage levels can be generated with the same configuration. The evaluation and performance investigation of CT-type is carried out with the alternate phase opposition disposition (APOD). The configuration and control approach has reduced the total harmonic distortion with high efficiency of output more effectively than other pulse width modulation techniques. The configuration and its control approach are executed on MATLAB/Simulink and the results are validated.**

***Index Terms*— CT-type MLI, APOD, THD, MATLAB, T-Type.**

I. INTRODUCTION

WITH the advent of power electronics, MULTILEVEL inverters (MLIs) are highly developed power electronics topologies in the modern era [1]. MLIs are created by combining various switch and source configurations and arrangements. These configurations of power electric switches can be used to produce different levels of outputs voltage. The immense capability of MLIs to improve the efficiency of the system has made them attractive for medium and high-power applications. Plug-in electric vehicles, renewable sources, batteries, and capacitors may all be easily interfaced using Multilevel., which is a stimulating element. [2].

The MLIs have many advantages over conventional inverters, including high voltage levels, low total harmonic distortion (THDs), and higher modularity. There are three categories for traditional MLIs, which are flying capacitor, neutral point clamped, and Cascaded H-bridge. With the above-mentioned topologies, with the increase in the number of level count harmonics are reduced which improves the power quality but the amount of electronic power switches required to design the above topologies is high and for control, each switch requires gate drives that make the system complex.

An MLI topology in [5][6] has been proposed in which fewer power electronic components are used, but the number of passive components, also sources is increased, making the crafts system less effective. Another interesting approach was implemented for the traditional MLIs to increase the level count. The unequal dc sources were introduced, known as asymmetrical topology, which amplified several levels. The greater number of levels of output voltage was achieved with the reduced switch count [8] but that increased voltage stress on power electronic switches. In [12] researcher proposed a new topology to get balanced voltages and decrease the voltage stress of switches.

The researcher in [15] implemented scheme with reduced switch count and achieved a higher number of levels with an asymmetrical arrangement. Although through this method with very few numbers of devices counts greater number of levels were achieved, the basic purpose of MLIs was violated due to the utilization of each switch which causes the high voltage rating. Performance analysis and mitigation of harmonics in the power system significantly improve the power quality being delivered to the consumers. So, this research gap motivated us to highlight the most appropriate method employing experimental investigation.

This paper proposes a CT-Type MLI topology that maximizes the output voltage with very high resolution. The configuration of the semiconductor device is done smartly to achieve desired levels with economical topology. The design of the proposed topology utilizes two back-to-back T-type modules to synthesize the nine-level output. The arrangement has eight power electronic switches with four equal dc sources. The core advantage of cross switched T type is that it does not use extra power electronic components to synthesize negative voltage levels. In the interesting configuration nine levels are produced in such a manner that four are positive, four are negative, and one is zero level. This smart approach not only reduces complexity but also works without a self-balancing bridge and reduces voltage stress.

II. WORKING PRINCIPLE OF CROSS-SWITCHED T-TYPE (CT) MULTILEVEL INVERTER

A. Module Configuration

The CT-type model is created by combining two T-type modules back-to-back. In each T-type module, there are two unidirectional switches, one bidirectional switch, and two dc

sources. The DC sources are wired so that their anodes do not come into contact with a positive DC supply, it ensures that diodes will not conduct. The bidirectional switches are required to block the current flowing from both polarities so that they prevent short circuits to occur. Each fundamental module produces three-level output. The fundamental modules are called L and R. The L and R modules of the T-type are connected back-to-back by two cross-connected switches. Each T-type modules have three points and are termed X, Y, and Z. The cross-connected switches are coupled with T-type modules. They are coupled in such a manner that the upper point of the L module is connected to the lower point (Z) of the R module. At the middle point of each module, the load is connected. The configuration is cleverly employed to generate a variety of output voltage levels since it uses fewer power electronic switches. The above-proposed circuit topology can easily be expanded to generate an increased level count, that reduce THDs to a significant value.

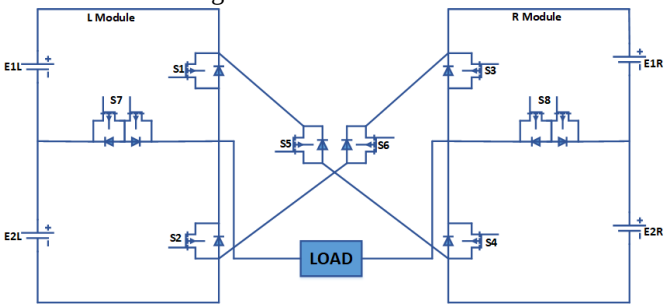

Fig 1: Proposed CT-Type MLI

B. *Working Principle of MLI*

As shown in figure 1, the configuration consists of four equal dc sources along with ten MOSFETs with feedback diode. the nine-level output voltage is obtained from the configuration. The above configuration is designed to assign different paths to current for each dc source. The circuit configuration does not involve additional H bridge circuitry to generate negative voltage as the dc sources of both modules are connected in such a way.to ensure the correct operation the switching arrangement is done in such a manner that the anode must not be connected with the positive terminal of the dc supply.it should also be ensured that the cross-connected switches do not operate simultaneously. In the symmetrical operation as mentioned earlier that the dc sources carry equal magnitude so (E1L = E2L = E1R = E2R = E. One of the benefits of the proposed scheme is that the switching elements for every polar level are identical. Consequently, the topology is termed a self-balancing bridge. The switches connected on the same arm (S1, S2) & (S3, S4) nor cross-connected switches (S5, S6) are not operated simultaneously. That results in the above configuration having some switching redundancies. This phenomenon is useful as reduced switching is possible with few changes in switching states, which are useful characteristics for space vector modulation.

C. *Development of Simulation Model of Proposed Topology*

The proposed configuration is implemented on the MATLAB Simulink. As shown in figure 2, the configuration contains eight switches among which two are bidirectional. Each switch requires a gate driver. The number of output levels can be raised by symmetrically increasing the dc sources. To calculate the number of levels, the equation is expressed as

$$N = 2n + 1 \qquad (1)$$

And the maximum gain can be obtained as

$$Vm = n * Vdc \qquad (2)$$

The number of levels is N, while the number of DC sources is n.

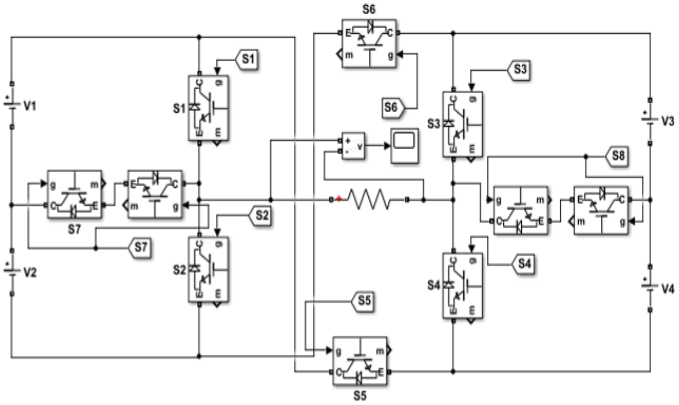

Fig 2a MATLAB Model Of CT-Type MLI

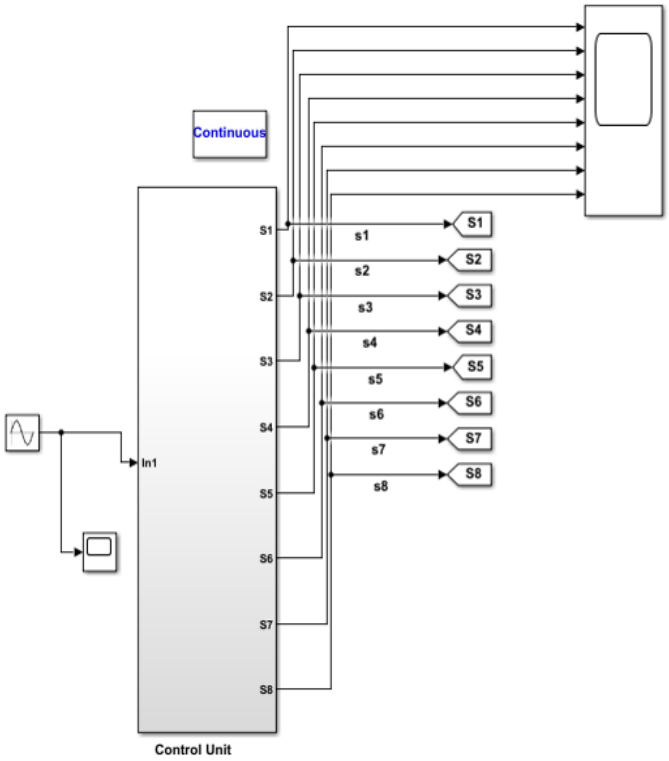

Fig 2b Control Unit of Proposed Topology

Modes	The various States Of Switching							
V_{BB}	$\dot{S}_1$	$\dot{S}_2$	$\dot{S}_3$	$\dot{S}_4$	$\dot{S}_5$	$\dot{S}_6$	$\dot{S}_7$	$\dot{S}_8$
4 E	✓	×	×	✓	×	✓	×	×
3 E(a)	✓	×	×	×	×	✓	×	✓
3 E(b)	×	×	×	✓	×	✓	✓	×
2 E(a)	✓	×	✓	×	×	✓	×	×
2 E(b)	×	✓	×	✓	×	✓	×	×
2 E(c)	×	×	×	×	×	✓	✓	✓
E (a)	×	×	✓	×	×	✓	✓	×
E (b)	×	✓	×	×	×	✓	×	✓
0 (a)	×	✓	✓	×	×	✓	×	×
0 (b)	×	✓	×	✓	✓	×	×	×
-E (a)	×	×	×	✓	✓	×	✓	×
-E (b)	✓	×	×	×	✓	×	×	✓
-2 E(a)	×	×	×	×	✓	×	✓	✓
-2 E(b)	×	✓	×	✓	✓	×	×	×
-2 E(c)	✓	×	✓	×	✓	×	×	×
-3 E(a)	×	✓	×	×	✓	×	×	✓
-3 E(b)	×	×	✓	×	✓	×	✓	×
-4 E	×	✓	✓	×	✓	×	×	×

TABLE I symmetrical Switching Pattern for different states

III. CONTROLLING SCHEME

To control the switching of MLI topologies mainly control techniques are classified into two categories namely high-frequency modulation and low-frequency modulation. PWM is a high-frequency modulation technique that includes anti-phase disposition (APD), anti-phase disposition (APD), carrier overlap (CO), and variable frequency (VF). [19,20,23,24]. For the proposed configuration CT-type MLI phase opposition disposition (POD) control scheme is carried out. In the POD (N-1), carriers are used to generate the N number of levels.

Alternate Phase Opposition disposition:

To generate nine-level from the proposed symmetrical configuration the APOD control scheme is implemented to produces a better harmonic spectrum. The configuration generated nine-level output so the number of carriers used is eight. Each carrier signal has a 1kHz frequency and the reference signal has a frequency of 50HZ. The carrier signal is compared to the reference signal as per switching in the APOD technique. In the APOD technique the switching signals are conjugates of the other signals. They are exactly out of phase of each other. In this topology there are eight switching signals.

The above control scheme is implemented on MATLAB SIMULINK to generate nine-level output. The switching pattern is illustrated below.

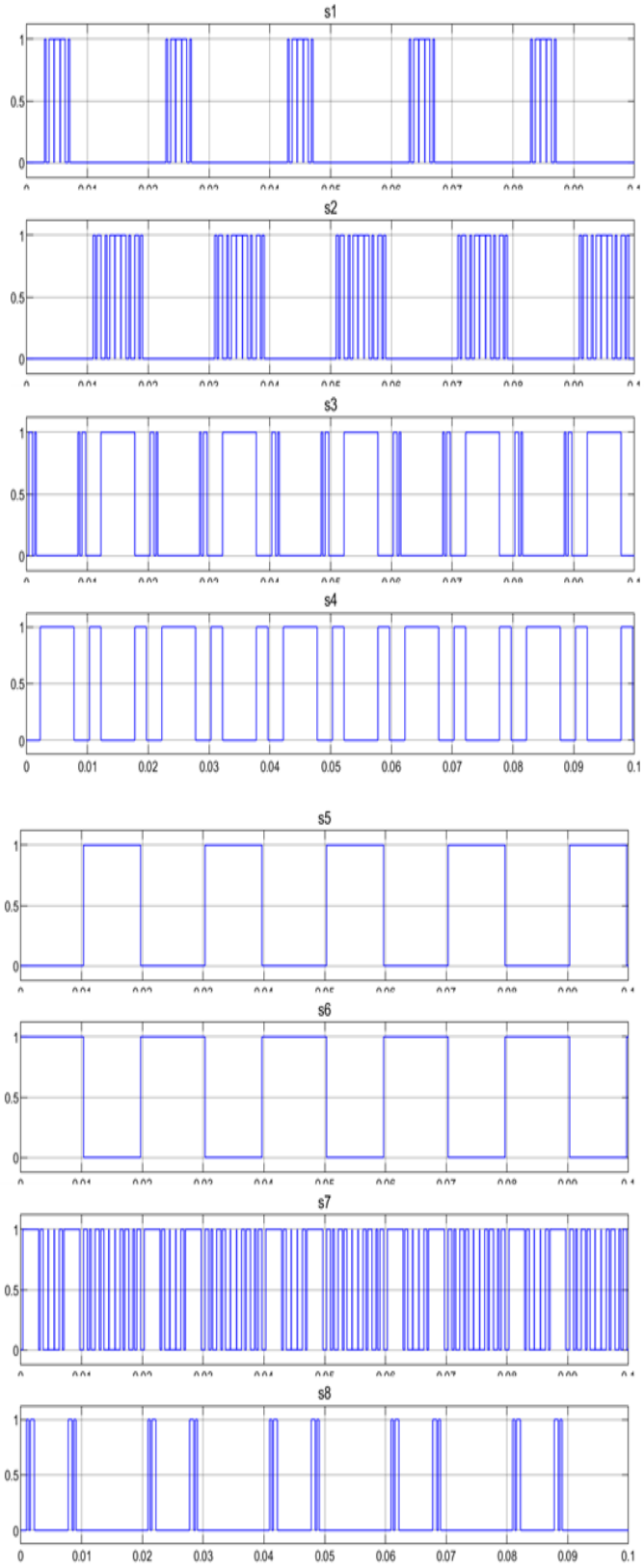

Fig 3 Switching Signals of POD Technique

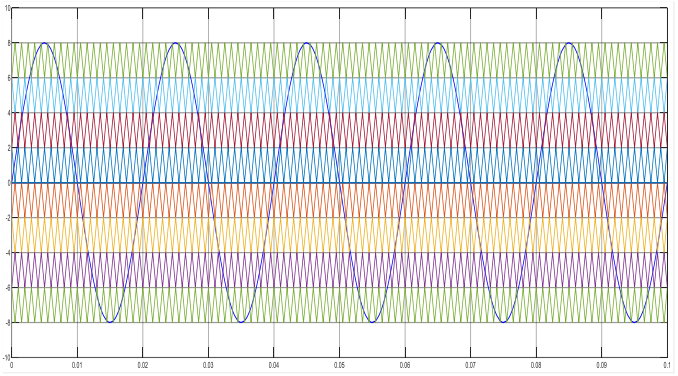

Fig 4 APOD Technique's Output

IV. Results and Discussion

As shown in figure 2, a simulation model was created using MATLAB/Simulink software to validate the results and analyze the performance of CT-type MLI. Table II shows the circuit parameters for the symmetrical operation. The model is executed and the results for the nine-level CT-type MLI are shown in figure 5. The fast Fourier transform (FFT) analysis is done to analyze the harmonic spectrum of output waveforms as shown in figure 6&7. The voltage levels used at L and R modules are equal, and the step size of staircase output will be equal to the E=10V. the maximum voltage obtained from the results is 40.1V, which validates the high performance of the configuration. The THD (total harmonic distortion) after implementing the control topology is reduced to 22.4% as shown in the figure 6. The harmonic distortion of the current has been reduced to the 6.69% as shown in figure 7. It is validated the CT-type topology has performed satisfactory performance with the APOD control scheme and the THD of the system is reduced to a greater extent with reduced complexity.

Configuration	Output Voltage	L Module	R Module
Symmetrical	39.97V	E1L = E2L = 10	E1R = E2R = 10

TABLE II: Parameters of CT-Type MLI

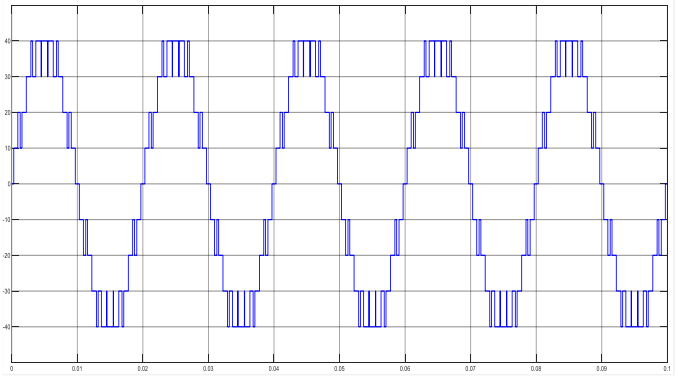

Fig 5 Nine Level Output of CT-Type

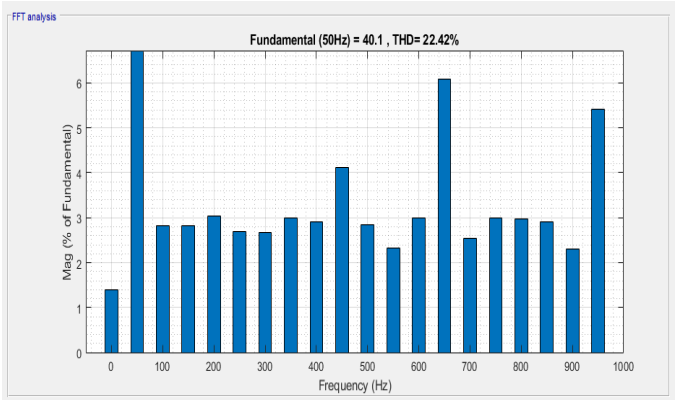

Fig 6 fast Fourier transform (FFT) Analysis of Output Voltage CT-Type Converter

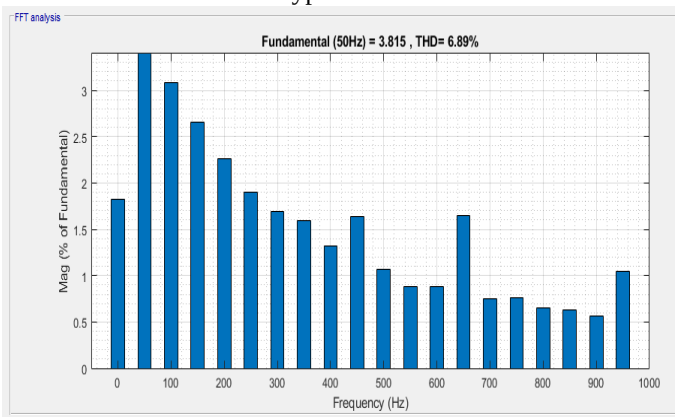

Fig 7 fast Fourier transform (FFT) Analysis of Current CT-Type Converter

V. Conclusion

The study presents the novel configuration of MLI to produce the high number of output levels named CT-type MLI. The setup is highly efficient and can be employed in a variety of high and medium applications. One of the foremost pros of CT-type is that it not only increases the reliability of the system but also reduces complexity, as negative voltage can also be generated from the same configuration without utilizing extra switches by only varying the switching states. The model can also be easily extended to generate a greater number of levels. It is also shown from the results that the THD of an inverter is reduced to a greater extent (22.4%). The symmetrical operation also introduces switching redundancies which are helpful during power failure.

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