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Design and development of hybrid multilevel inverter

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Abstract **—It is known that the Multilevel Inverter (MLI) topology is an appealing one for high voltage DC-AC conversion. This research paper presents a hybrid multilevel inverter model based on MATLAB/SIMULINK. It is made up of a nine-level inverter. Reduced switch counts, greater level generation with fewer sources, and the potential for higher level generation with fewer component counts are just a few of the many benefits of the suggested architecture. MATLAB/SIMULINK is used to construct the control model and the main circuit model. We experimentally examine a nine-level hybrid multilevel inverter. To reduce harmonics, selective harmonic elimination (SHE), is used. The simulation provides a reliable approximation of the inverter test findings. Through the integration of simulation and hardware experimentation, this study provides a thorough foundation for the future implementation of hybrid multilevel inverters in real-world power systems, in addition to validating their efficacy.**

Index Terms**— Multilevel Inverter (MLI); Hybrid Multilevel Inverter; DC-AC Conversion; Selective Harmonic Elimination (SHE); MATLAB/SIMULINK.**

I. INTRODUCTION

Modern and widely used kind of power electronic converter is the multilevel inverter, which creates a specified output voltage by using many levels of dc voltages as inputs. It is possible to synthesize a nearly sinusoidal voltage waveform with a sufficient number of dc sources [1]. Traditional multi-level inverters have limitations, including a higher number of components, leading to increased cost and reduced reliability, Complex control strategies, requiring advanced algorithms and processing power, Reduced efficiency, due to switching losses and conduction losses. In comparison to traditional MLI, it offers a number of benefits, including transformer less construction, reduced switching loss, low power switch stress, and high power quality signal. However, the harmonics issue poses a hurdle to this technology and has negative impacts on several applications. Low-order harmonics are the most harmful to the system because they induce torque spikes in the electric actuators, which lower system life and reduce efficiency [2-3]. Comparing the two-level inverter with The reduction of parts such switches, control circuits, voltage source capacitors, and diodes is the primary benefit of MLI. In addition, there are low harmonic components, voltage ripple, low switching loss and high power quality [4]. This study aims to advance this trajectory by exploring the complex synergy between Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) techniques in the field of multilevel inverters. Switching angles at different fundamental frequency for a multilevel inverter are achieved by solving the selective harmonic elimination equations in a way that produces the intended fundamental voltage and eliminates some lower order harmonics. Due to the nonlinear transcendental character of these equations, a given modulation index may have a single, numerous, or even no solutions [5]. The use of Selective Harmonic Removal (SHM) is made to improve harmonics. The SHEPWM method is used to optimize the step-harmonic waveform for multi-level inverters by genetic algorithm. It involves solving sets of nonlinear transcendental equations that represent the relationship between the fundamental wave amplitude, harmonic components, and commutation angle. Hybrid multi-level inverters (HMLIs) have been proposed as a solution to address these limitations.

II. METHODLOGY

A. Block Diagram of Hybrid Multilevel Inverter

The block diagram of the hybrid multilevel inverter is shown in figure 1. There are total four equal DC voltage supply of each 12 volts. The circuit comprises of 16 MOSFET switches.

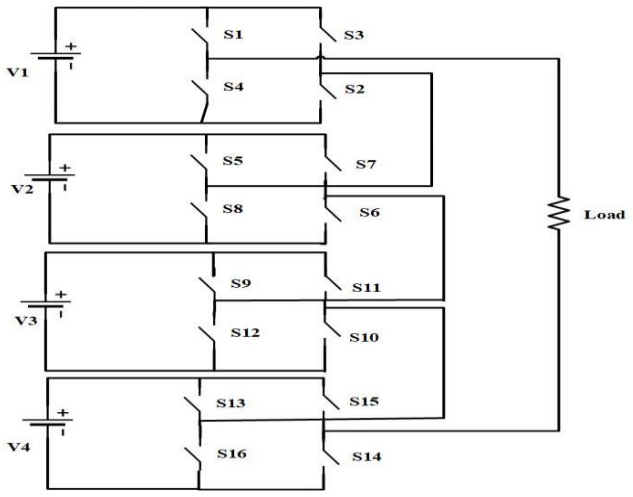


Fig.1.Hybrid multilevel inverter

To find the different parameters of proposed system followings equations are given

The overall voltage magnitude of multilevel inverter is given in eq. (1) **[6-7]**

$$V_{out} = \sum V_n = V_1 + V_2 + V_3 + V_4 \qquad \textbf{(1)}$$

The number of effective output voltage levels is given in eq. (2)

$$N_L = 2K + 1 \quad \textbf{(2)}$$

The number of switches is given in eq. (3)

$$N_{SW} = (N_L - 1) \times 2 \quad \textbf{(3)}$$

The number of DC sources is given in eq. (4)

$$N_{DC} = \frac{(NL-1)}{2} \quad \textbf{(4)}$$

Where,

N_{DC} is the number of DC sources.
N_{SW} is the number of switches.
N_L is the voltage levels .
K is the number of H-bridge units.

B. Switching Scheme

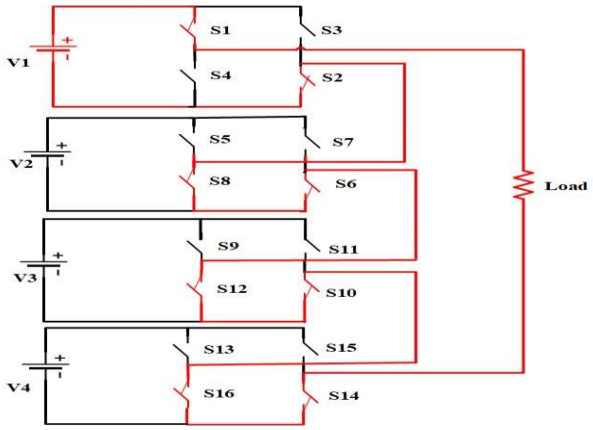
A switching table for a MLI is a critical component that dictates how the inverter switches should operate to produce the desired output voltage levels. The switching table is shown in table 1. During state 1the switches $S_1, S_2, S_6, S_8, S_{10}, S_{12}, S_{14}, S_{16}$ are closed while $S_3, S_4, S_5, S_7, S_9, S_{11}, S_{13}, S_{15}$ are opened with output voltage of 1V.In the same way for state 2, the switches $S_1, S_2, S_5, S_6, S_{10}, S_{12}, S_{14}, S_{16}$ are closed while switches $S_3, S_4, S_7, S_8, S_9, S_{11}, S_{13}, S_{15}$ are opened with output voltage of 2V.In the same way for states 3,4,5,6,7,8,9 respective switches are turned on and off.

TABLE I: Switching scheme of hybrid MLI.

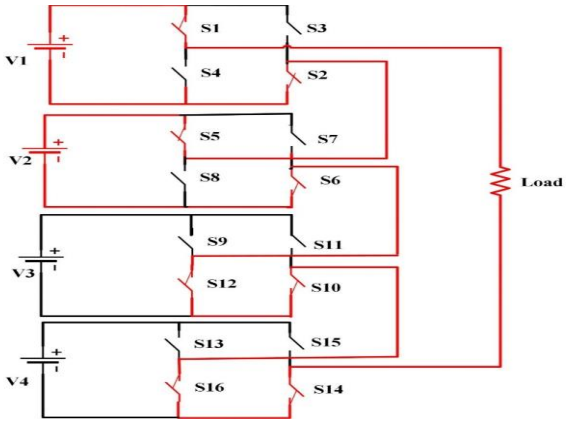
state	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	s_9	s_{10}	s_{11}	s_{12}	s_{13}	s_{14}	s_{15}	s_{16}	v_{out}
1	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	1V
2	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	2V
3	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	3V
4	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	4V
5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0V
6	0	0	1	1	0	1	0	1	0	1	1	0	0	1	0	1	-1V
7	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	1	-2V
8	0	0	1	1	1	1	0	0	1	1	0	0	0	1	0	1	-3V
9	0	0	1	1	1	1	0	0	0	0	1	1	0	1	0	1	-4V

C. Switching Modes

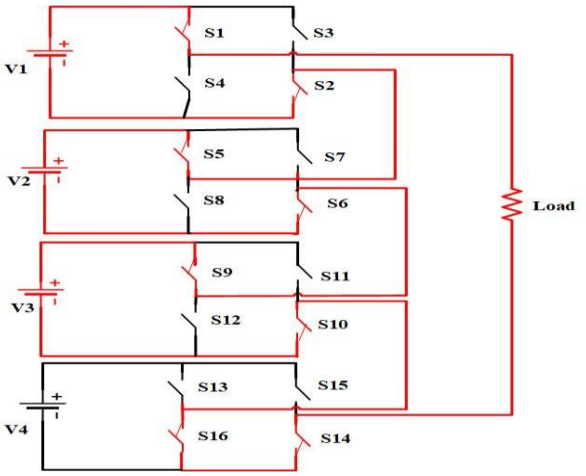
Switching modes for hybrid MLI are shown in figure 2. switching modes. Each switching mode corresponds to a specific arrangement of semiconductor switches (such as IGBTs or MOSFETs) within the inverter topology. For example, in a cascaded H-bridge multilevel inverter, each H-bridge module can be controlled independently to achieve different output voltage levels. The switching modes in this case would refer to the various combinations of switching states for the semiconductor switches in each H-bridge module.



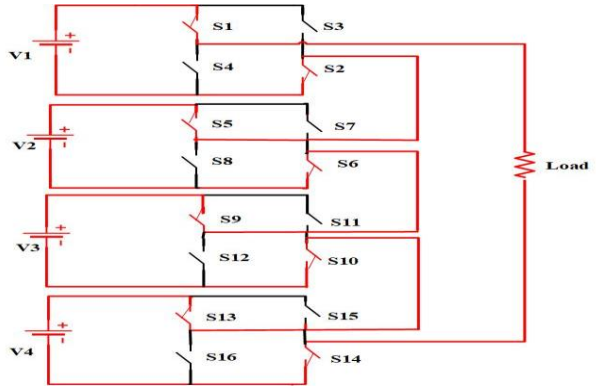
(a)+1VDC



(b) +2VDC



(c)+3VDC



*(d)+4*VDC

Fig. 2.Switching modes

III. SYSTEM DESIGN

A. Simulation model of Proposed System

Figure 3 shows the simulation model of proposed system. It consists of four subunits of H bridges. Each subunit consists of equal magnitude of 12V. The components connected in this proposed model are given by figure 3.

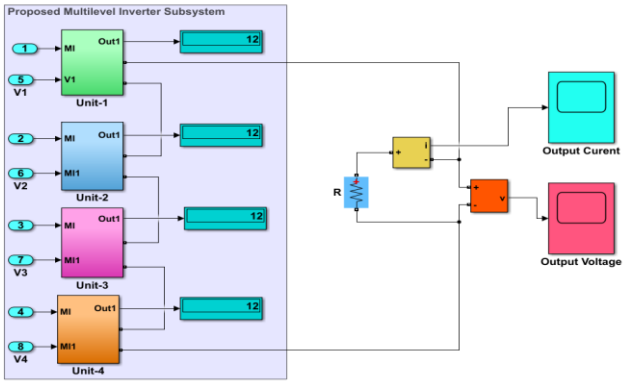


Fig.3.Simulation Model of Proposed System

B. Simulation Model of Subunit

In a hybrid multilevel inverter that incorporates a subunit with four MOSFET switches and a load resistor, control techniques play a crucial role in managing the switching of the MOSFETs to produce the desired output voltage. The load resistor serves several important functions, such as balancing voltage levels across different stages of the inverter, damping oscillations that. occur during switching, and limiting current in case of faults to protect the system. Additionally, it helps dissipate excess energy safely during transients and aids in testing and calibration by simulating real load conditions. Selective harmonic elimination is one way used to control the MOSFET switches. Pulse width that adjusts the switches' duty cycle to create the appropriate voltage waveform and reduce harmonic distortion. The components connected in sub unit are given in figure 4.

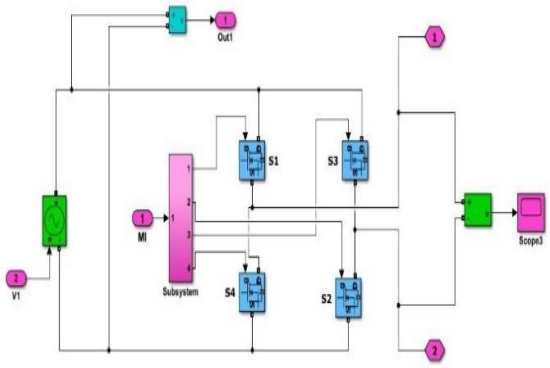


Fig.4. Simulation model of subunit

C. Simulation Model of Control Circuit

In multilevel inverters (MLIs), selective harmonic elimination (SHE) techniques are commonly utilized to calculate switching angles in a way that simultaneously eliminates the dominating low order harmonics and yields the desired fundamental output voltage.

It is possible to reduce the THD and the output filter's size in SHE. Since the switching angles are predefined off-line, the modulation technique is thought to be open-loop [8,9].

The SHE's essential duties include (i) preserving the waveform's basic element; (ii) Individual harmonic reduction; (iiia reduction in THD, and (iv) reduced switching losses. To minimize the lower-order harmonics, the SHE approach necessitates the creation of large passive filters, which is a significant downside. [10]. Researchers have presented a unique strategy in the literature called selective harmonic mitigation (SHM) to address the aforementioned issue with the SHE method [11].

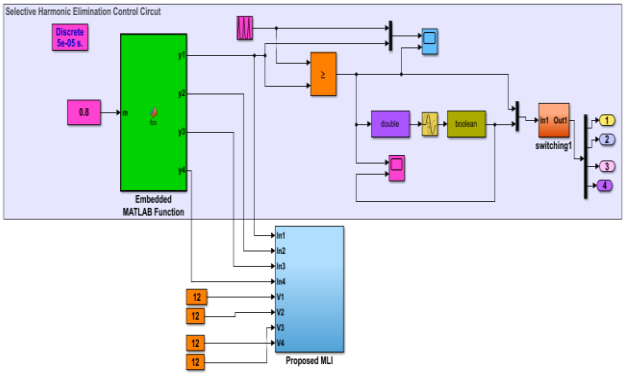


Fig.5.Simulation Model of Control Circuit

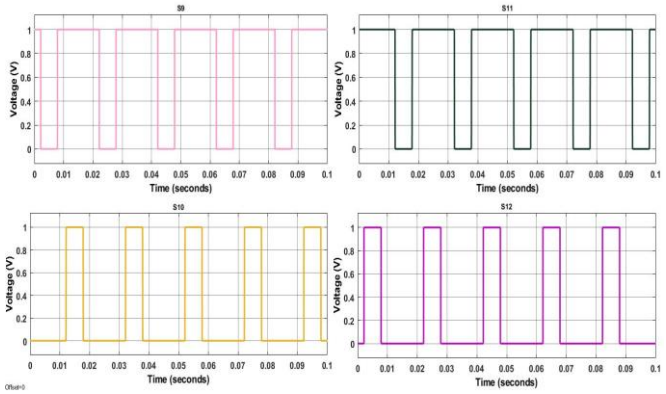
IV. SIMULATION RESULTS

The simulation's waveforms, which are displayed below, reveal the outcomes of the hybrid multilevel inverter with selective harmonic removal and the multilevel inverter's THD. In multilayer inverters (MLIs), selective harmonic elimination (SHE) techniques are commonly utilized to calculate switching angles in a way that simultaneously eliminates the dominating

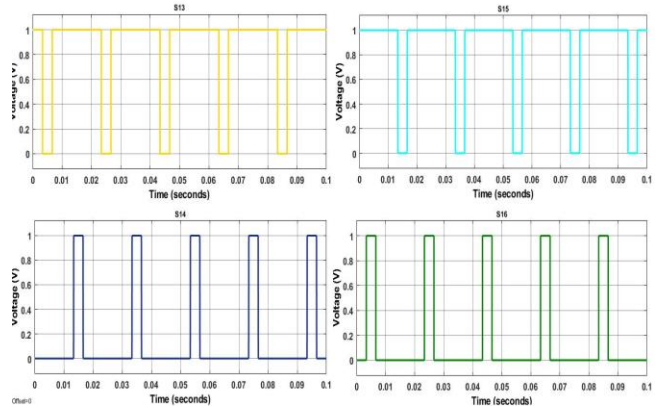
low order harmonics and yields the desired fundamental output voltage.

A. Simulation Results Of Selective Harmonic Elimination Technique

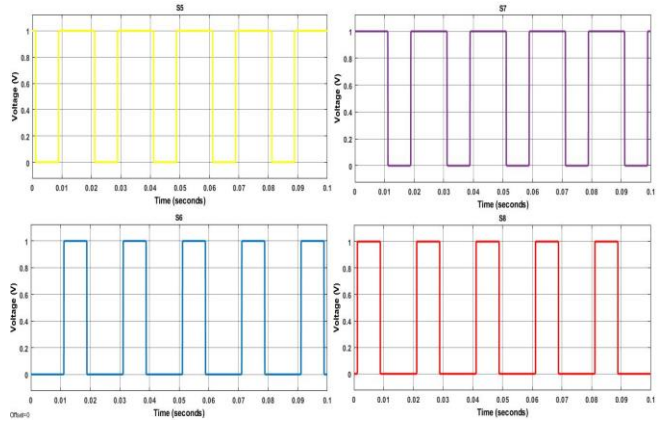
Control signals to MOSFET switches in a multilevel inverter are essential for managing the timing and sequence of switching actions to generate the desired output waveform. MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) are voltage-controlled devices. The voltage applied to the gate terminal V_{GS} relative to the source terminal determines whether the MOSFET is in the "on" state (conducting) or "off" state (non-conducting).



(a)



(b)



(c)

Fig 6.Control Signals To Switches

B. Output Voltage of Multilevel Inverter

The output voltage of the proposed MLI is 48V and output current is 0. 48 A by using four symmetric DC voltage sources is given by figure 7 shown below.

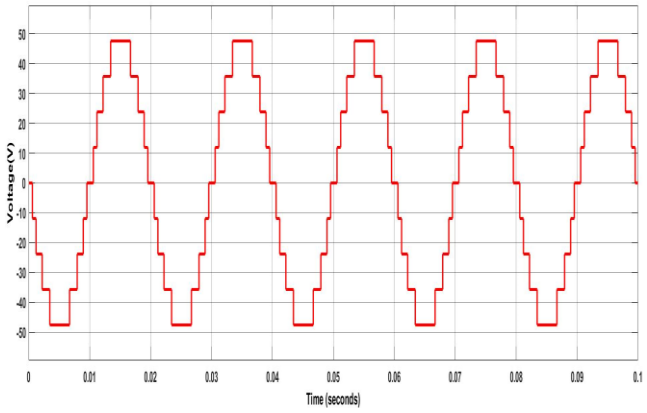


Fig.7.Output voltage

C. Output current of Multilevel Inverter

The output current of proposed MLI is 0. 48 A .In the figure 8 shown below contains x axis on which time is given and on y axis current is given .

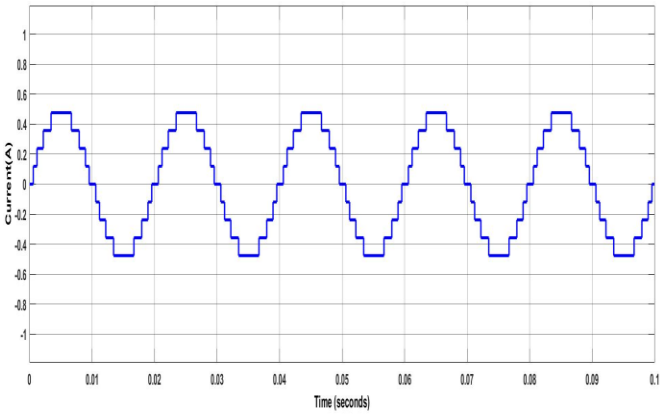


Fig. 8. Output current

D. Total Harmonic Distortion

The ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency is known as the total harmonic distortion (THD), which is a measurement of the harmonic distortion present in a signal.

$$\mathrm{THD_F} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots}}{V_1}$$

where Vn is the RMS value of the *n*th harmonic voltage and V_1 is the RMS value of the fundamental component. Total

harmonic distortion of proposed MLI is found to be 9.63% as shown in figure 9.

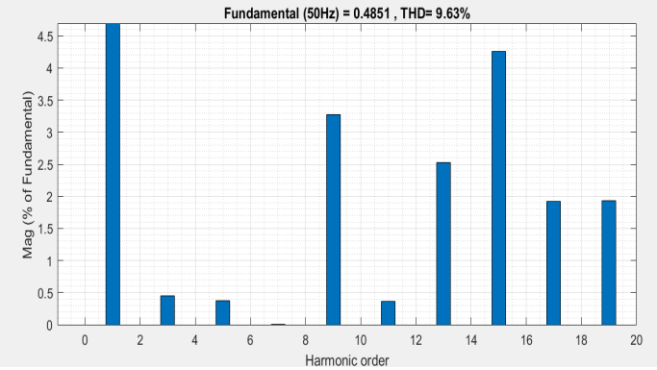


Fig.9. Total Harmonic Distortion

V. HARDWARE IMPLEMENTATION

The Hardware model of hybrid multilevel inverter consists of a batteries, loads, buck converter, inverter, step up transformer, 4 MOSFET bridges ach bridge consist of four bridges and power line. The experimental setup is shown in figure 10.

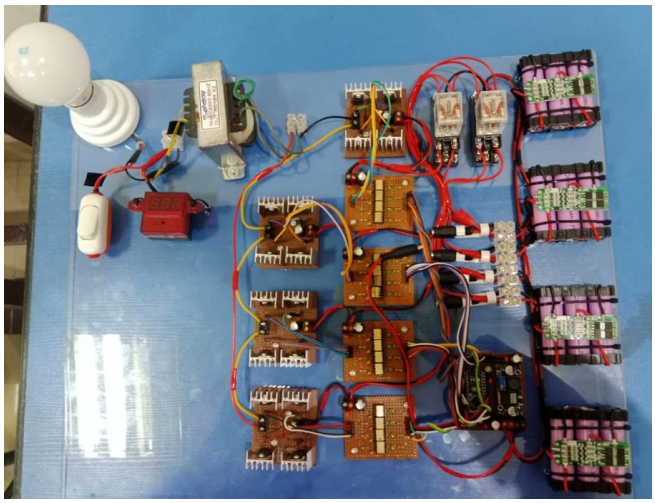


Fig.10. Nine Level Hybrid MLI

VI. HARDWARE RESULTS

A. Output Voltage

The below figure 11 and 12 shows the output voltage waveform and output voltage of hybrid multilevel inverter in which 9 levels are generated. The total output voltage is found to be 37.17 volts as shown in figure 12. The hardware is tested on different loads. At load 1 which is 2W we get voltage regulation of 0.7%and at load 18W we get voltage regulation of 14.5% and so on

Fig. 11. Output voltage waveform

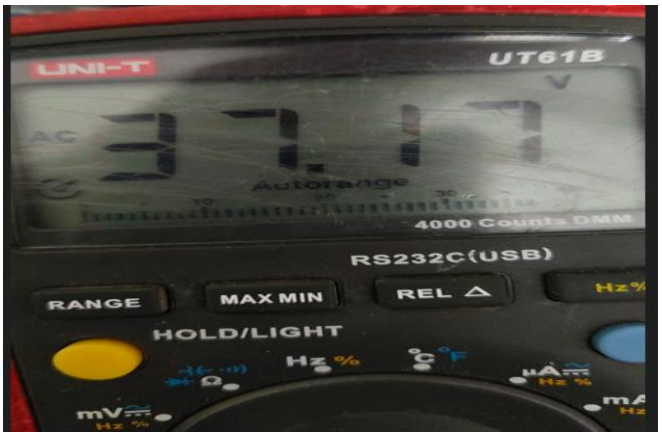


Fig.12. Output Voltage

VII. CONCLUSION

A single-phase nine-level hybrid multilevel inverter (MLI) is designed in this research work. The proposed topology has minimum components compared to the other conventional topologies. It consists of 16 switches and 4 DC sources. This proposed model is simulated in MATLAB with Selective Harmonic Elimination (SHE) technique to reduce harmonics. The simulation shows an output voltage of 48V, current of 0.48 A, and total harmonic distortion (THD) of 9.63%. Hardware model is also designed in this research work. For the hardware implementation, each DC voltage source is equal to 12V.The model is tested on different loads and the voltage regulation is found to be 0.7%.and 14.5%. The hardware implementation delivered good results, with an output voltage of approximately 37.17 V. It shows that hardware model effectively generates nine voltage levels with minimum components.

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