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Modeling and Field Oriented Control of Permanent Magnet Synchronous Motor Using FPGA

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***Abstract* — In this paper a simple and rapid prototyping approach for PMSM motor drives using MATLAB/Simulink and HDL Coder is presented. The Simulink model of PMSM based on the dq structure and principle of field-oriented control (FOC) is developed and simulation results are presented. The proposed model is optimized and converted to VHDL code for FPGA deployment which eliminates difficult, error prone and time-consuming manual coding. The FOC current algorithm for PMSM is implemented inside Xilinx Virtex5 FPGA using the HDL Coder. The FPGA implementation of the overall controlling algorithm using HDL coder has certainly reduced the execution time significantly as compared to DSP based controllers thus increasing the productivity and opportunities to design more complex control algorithms in relatively short time. Besides this, proposed design is validated with the existing works. The implementation results reveal that the proposed field oriented controller takes only 20.875 ns of execution time with 47.945 MHz clock, which is the lowest and optimum calculation period for the era.**

***Index Terms*— FPGA, Field oriented control, Hardware description language coder, Permanent magnet, Synchronous motor.**

I. INTRODUCTION

With the advancement of permanent magnetic materials, computing technology and power electronics, ac motors, especially PM synchronous motors are adopted by many industries. The reasons are their many undisputable advantages such as good efficiency, high accuracy and reliability, low cost, high power density, easy maintenance. In spite of the various high-performance applications of PMSM, its control is very challenging and has engaged the attention of many researchers [1, 2].

In order to achieve better dynamic performance, more complex and sophisticated techniques are needed to control the PM motor. Field Oriented Control is a type of vector control which provides closed loop control of PMSM. Having closed loop control provides great control over the motor [3]. FOC technique includes three reference frames and requires two transformations from one to the other to decouple the torque and flux producing currents, which leads to the structure similar to the dc motor [4]. To achieve optimal efficiency of the servo drives, the implementation of FOC needs fast and highly accurate controllers. Field programming gate array are commonly used as hardware implementation platform for such control application. FPGAs have become optimal selection owing to their outstanding characteristics such as re-configurability, parallelism, optimization, high performance, low computational power, low cost etc., which make them one of the best candidates for implementing high performance motor-drive (control) application [5,6]. All the logic inside the FPGA can be programmed to acquire desired design using hardware description language (HDL). Two mostly used HDL are Verilog and VHDL. Manual coding of design is difficult, having possibility of human error and requires long time period. The MATLAB/Simulink environment provides HDL Coder tool to be used for automatic HDL code generation for rapid system development. This methodology is faster, enables designers to make changes in the design at the system level, and can generate an optimized HDL code easily.

This research presents an effective approach for FPGA implementation of Field oriented control algorithm of PMSM motors using HDL Coder within MATLAB/Simulink environment.

II. LITERATURE REVIEW

Field Oriented Control of PMSM drives have been extensively studied in the literature. Several researchers have implemented the digital signal processor based current controllers in FOC PMSM drives. A number of papers have been written for implementation of FOC control for PMSM drives in FPGA technology. A brief review of related work is given as under:

Samat, et al. [8] present DSP based PMSM controller based on FOC method. The system is implemented using a TMS320F2808 DSP controller. They have performed various mode of operation to follow the reference speed to give high performance drive system. Zhang, et al. [9] have designed the mathematical model of Field Oriented Control of PI controller for PMSM in Simulink. Skiwski, et al. [10] has presented PMSM drive based on STM32F4 microcontroller by applying the field-oriented control (FOC) technique to ensure the high performance operation of PMSM. Synthesis procedure of controllers has been made in Matlab/Simulink environment. The results prove proper operation of the drive in torque and speed mode. Wang, et al.[11] have proposed the combine strategy of field oriented control and sliding mode control (FOSMC) on permanent magnet AC motors, to improve the overall performance in terms of torque and speed and enhanced the load variations and uncertainties in the model. They have implemented and compared both first and higher orders FOSMC of surface mounted permanent magnet AC motors and found that higher order FOSMC has better performance by providing less oscillatory dynamic response thus faster transient response. The hardware implementations are carried out using a Texas Instruments TMS320F28335 DSP based prototype platform. Gao, et al. [12] has presented the design and implementation of the PMSM drive based on the IGBT intelligent power module. The vector control principle is used along with space vector modulation technique as control methods. The hardware is implemented using TMS320F28377S DSP and IGBT power module.

Many researchers have studied and proposed FPGA based implementation of FOC control of PMSM drives to deal with the time constraints.

Naouar, et al.[13] present FPGA implementation for current controller of synchronous speed drive system. Spartan3 XC3S400 FPGA has been used for this purpose. Marufuzzaman, et al. [14] have presented FPGA based solution of current dq PI controller. This implementation is modeled in Quartus II Altera environment and the results show that FOC controller implementation requires minimal calculation time i.e. 50ns. Lai, et al. [15] present FPGA based vector control hardware current loop controller for a PMSM drive using MATLAB/Simulink. The developed system is developed in Verilog and implemented on an Altera FPGA device. Ramirez, et al. [16] have developed and evaluated a sensor less implementation of PMSM based on FPGA at low range speed using predictive scheme with variable switching frequency using FOC approach. The results have shown faster execution and operation at lower speed range without the need of a signal injection.

From the literature review it is found that, traditional PMSM controller systems are based on digital signal processors. The performance of motor drives with DSP based controllers is limited by hardware structure and computing capacity due to its sequential processing. In order to speed up the calculation time to attain fast response reconfigurable hardware in the form of FPGA is considered as a practical way of achieving high performance FOC of PMSM drives with good accuracy. The FPGA based digital designs that use hardware description languages require preliminary knowledge and skills in the tools such as VHDL and Verilog. This work presents an effective methodology for Field oriented control of PMSM drives into a FPGA platform with MATLAB/Simulink using HDL Coder.

III. MATHEMATICAL MODEL OF PMSM

Mathematical model of PMSM derive in the d-q coordinate based on rotor flux oriented control method, is given as [7,16]:
The stator voltage equation can be obtained as:

$$V_d = R_s i_d + p\ \psi_d - \omega_r\ \psi_q \quad (1)$$

$$V_q = R s i_q + p\ \psi_q + \omega_r\ \psi_d \quad (2)$$

Flux linkages are given by

$$\psi_d = L_d i_d + \psi_r \quad (3)$$

$$\psi_q = L_q i_q \quad (4)$$

By substituting equations 3 & 4 into 1 and 2:

$$V_d = R_s i_d + p\ (L_d i_d + \psi_d) - \omega_r L_q i_q \quad (5)$$

$$V_q = R s i_q + p L_q i_q + \omega_r (L_d i_d + \psi_r) \quad (6)$$

The developed torque equation is given as:

$$T_e = \frac{3}{2} \mathrm{P}\ (\psi_d i_q - \psi_q i_d) \quad (7)$$

$$= \frac{3}{2} \mathrm{P}\ [\psi_r i_q + (L_d - L_q)\ i_d i_q] \quad (8)$$

The mechanical torque equation is given as

$$T_e = T_L + B\omega_m + \frac{Jd\omega_m}{dt} \quad (9)$$

The rotor mechanical equation is obtained by rearranging equation (9):

$$T_e = \frac{\int (T_e - T_L - B\omega m)}{j} \quad (10)$$

And $$\omega_m = \omega_r \frac{2}{\mathrm{P}} \quad (11)$$

IV. DESIGN METHODOLOGY

The overall workflow of design is given in Fig.1. The proposed approach of design is an alternative to traditional FPGA design flow using manual HDL coding which is difficult, time taking and error prone. This model based design at system level shortens the developing, debugging and validation time. Methodology includes designing of FOC current controller model for PMSM in MATLAB/Simulink. After that Simulink model of FOC algorithm is prepared and configured to be used by HDL coder for code generation. Once the configuration and parameters setting of model is accomplished, then using HDL Workflow Advisor, VHDL code of design is generated. Generated VHDL code is synthesized for hardware realization and implemented on FPGA Virtex 5 device.

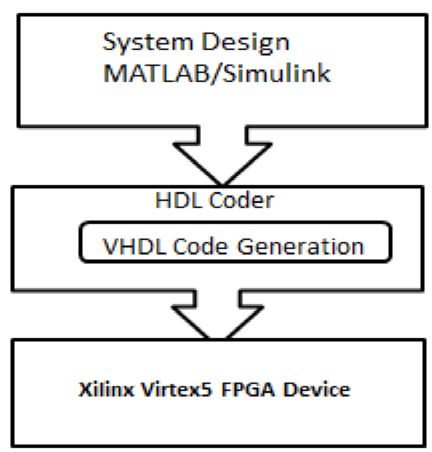

Fig. 1. Design work flow

V. SYSTEM DESIGN

The overall Simulink model of the system as shown in Fig. 2 contains current controller and motor modules are discussed in subsequent sections.

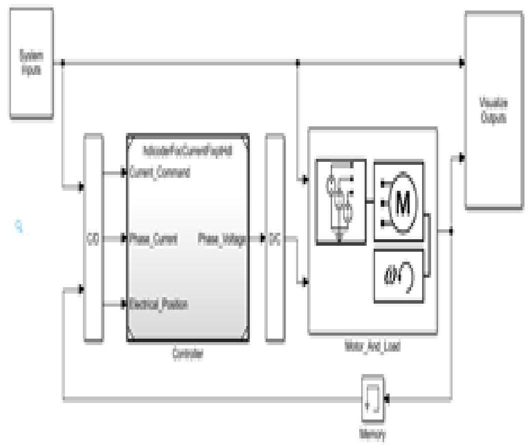

Fig. 1. Simulink model of field oriented control of PMSM

A. Field Oriented Control (FOC) Current Controller

The current controller module is mainly designed to generate motor currents according to system inputs. The FOC module contains Park and Clarke transformation, D-Q current control, and Inverse park and Clarke transformation, Space vector modulation as shown in Fig.3. The main principle of FOC is to control the torque and flux separately. In order to ease the individual control, first two transformations take place. The motor phase currents are transferred from the three phase balanced **sys**tem $(\mathbf{I_a, I_b, I_C})$ into 2- ϕ balanced system $(\mathbf{I_\alpha, I_\beta})$ by means of Clarke Transformation**.** Further by using Park transformation the 2-ϕ system is remodeled into rotating 2- ϕ system $(\mathbf{I_d}$ & $\mathbf{I_q})$ [7]. The SinCos block does the calculations of the sine and cosine values for the angle passed through it which actually is the rotor angle (electrical position P). It gives the sine and cosine values to the park transformation block and help in controlling the motor currents by FOC (field oriented control). After that the resultant parameter is controlled using PI controller. PI controller is designed individually for both d and q control. Voltage modulation index (VMI) command is the output from the current PI controller, which is sent to the SVPMW module after being evaluated. D-command from Clarke transformation is set to 0 because d refers to the flux and setting any value of flux will ultimately increase operating speed. In this research operating frequency is not increased, thus the "d" is set to 0.

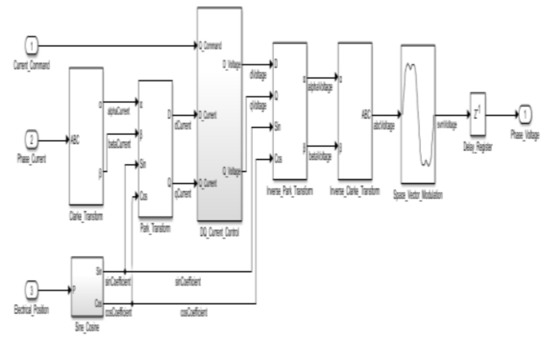

Fig. 3. Detailed view of FOC

B. Permanent Magnetic Synchronous Motor Model

Using SimPower Systems library tool, Simulink model of PMSM motor is developed. The PMSM motor block models a permanent magnet synchronous motor with a three-phase wye-wound stator having sinusoidal flux distribution and is created according to the Equations 1 to 6 given in Section 3. The PMSM motor model is shown in Fig.4

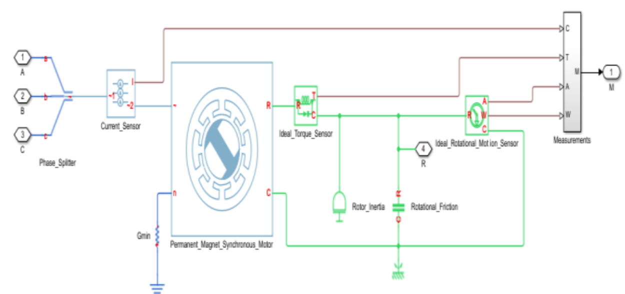

Fig. 4. Permanent Magnetic Synchronous Motor

According to parameters of the interested PMSM motor, module can be manually configured. The motor parameters of module are configured according to the specifications given in Table 1.

Table 1: Motor Specifications

Parameter	Value
Rated Voltage V	24 V
Rated Speed S	418.87902047863906 rpm
Maximum Current Imax	5.4 A
Voltage max Vmax	24 V
Poles pairs P	4
Stator resistance	0.9 ohm
d-axis Inductance L_d	0.00105 H
q-axis Inductance L_q	0.00105 H
Zero Sequence Inductance L_0	0.00105 H
Flux Linkage ψ	0.005661 Wb
Inertia J	2.40092768E-6 kg.m^2

VI. FPGA PROGRAMMING

After designing the Simulink model of Field oriented controller for PMSM, the design is modified to meet the requirements of the HDL Coder. Fixed-point data conversion is done during the process of VHDL code generation in order to reduce hardware resources. Moreover, a word-length and fraction length optimization of the fixed-point data is one of critical phase of algorithm implementation on a FPGA. To achieve fixed-point model of FOC algorithm which corresponds to floating-point, WL (Word Length) and FL (Fraction Length) values of 16 and 8 are chosen from fixed point optimization process using HDL Workflow Advisor of the HDL Coder [21]. Once the conversion process is completed and Simulink model of design is successfully converted into hardware design, generated VHDL code of FOC algorithm is processed in Xilinx ISE 14.2 software for synthesis and implementation on Virtex5 xc5vlx50t-ff1136 FPGA device.

VII. RESULT AND DISCUSSION

The Simulink model of FOC current control algorithm is simulated in MATLAB/Simulink environment. An extensive simulation studies were conducted and consistently good results have been obtained. The aim of the work is to deal flux and torque components of current independently of each other to achieve the optimal control of PMSM. Using FOC control technique the quadrature current is generated which controls the torque so that maximum torque can be achieved. As an example, gain value of K_p = 8 and K_i =2000 are used and step current command of 2A is given and the load velocity changes between locked rotor (zero), +150 rad/sec, and -150 rad/sec as shown in Fig. 5.

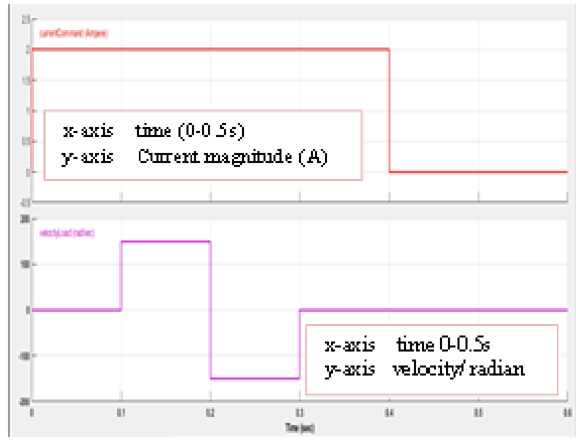

Fig. 5. Current command and measured and load velocity of PMSM.

The three phase current applied to the PMSM are shown in Fig.6. After passing through Clark and Park transformation blocks, alpha axis current (**$I_{s\alpha}$**), beta axis current (**$I_{s\beta}$**), direct axis current (**I_d**) and quadrature axis current (**I_q**) are obtained as shown in Fig.7 and 8 respectively.

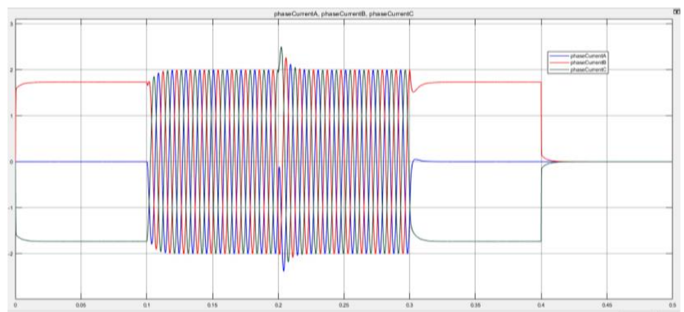

Fig. 6. 3-phase imput supply current of PMSM

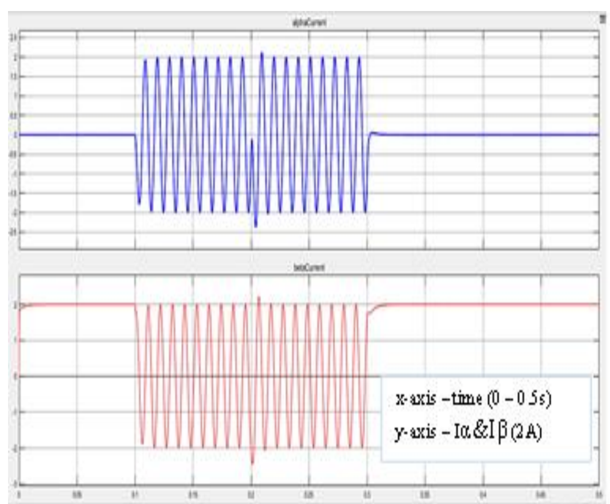

Fig. 7. Alpha current (I_α) & beta current (I_β) after Clark Transformation

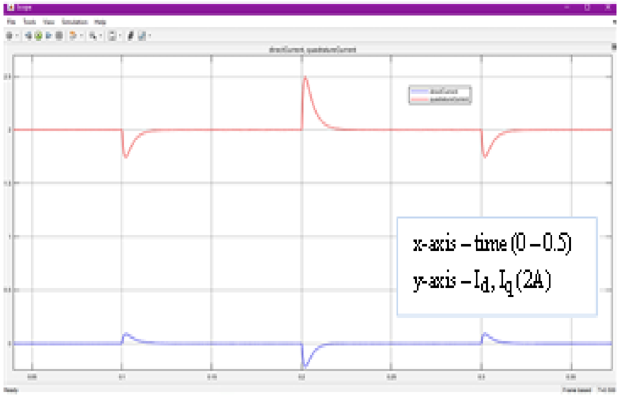

Fig. 8. Direct current (**I_d**) & quadrature current (**I_q**) after transformation

We get two phase 90° displaced rotating reference frame with **I_d** & **I_q** currents after transformation. The **I_d** current is defined as field weakening current on the x-axis with zero amplitude, where the **I_q** current in plot, is at the value relative to current command. It can be seen from the Fig.9 that the waveform of quadrature current is nearly same as electromagnet torque which shows that the electromagnetic torque closely follows the measured quadrature current of the motor using the gain value of $K_p = 8$ and $K_i = 2000$.

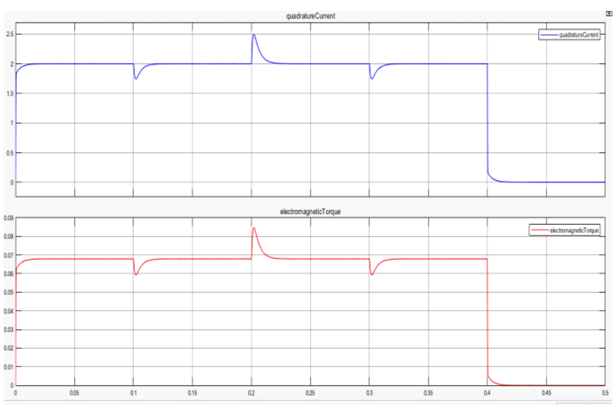

Fig. 9. Quardrature currrent and electromagnet torque of PMSM

VIII. IMPLEMENTATION RESULTS

The proposed design of FOC current controller is implemented on Virtex5 xc5vlx50t-ff1136FPGA target device using Xilinx ISE Design Suite 14.2. The design utilization summary of the proposed FOC current controller of PMSM is shown in Table 2. From the table it is observed that proposed design occupies 64 slice registers, 1167 look up tables and 148 bonded Input outputs of the device. Hence a small chunk of FPGA resources (i.e. < 5%) is used by the model. As the hardware consumption determines the cost of any design, the proposed design utilizes less hardware and thus it is cost effective. Table 3 shows the timing performance of the design. The hardware implementation of the controller has clock speed of 47.945MHZ with the minimum period of 20.857ns.

Table 2: Device Utilization Summary

Slice Logic	Available	Used	Utilization
Number of slice registers	28800	64	1%
Number of Slice LUTS	28800	1167	4%
Number of fully used LUT-FF pairs	11,67	64	5%
Number of bonded IOBs	480	148	30%
Number of block RAM/FIFO	60	-	-
Number of BUFG/ BUFGCTRLS	32	1	3%
Number of occupied Slices	7,200	364	5%

Table 3: Timing Performance

Parameter	**Value**
Minimum period	20.857ns
Maximum frequency	47.945MHZ
Speed Grade	-2

Table 4 shows the comparison of implementation results of the proposed work on a FPGA platform with previous works. Although it is no easy to make comparison since the approach used for the algorithm is changed and also hardware implementation technique and the device on which implementation is done is different. It can be noted that proposed design takes less hardware utilization time. The design working with an estimated speed of 47.945MHz frequency is more than enough for FOC controller of PMSM drive.

Table 4: Comparison of implementation results of the proposed work on a FPGA platform

Work	Siwakoti et al. (2013) [20]	Marufuzzaman et al. (2014) [13]	Chiu-keng Lai et al. (2017) [14]	Wencong Tu et al. (2019) [21]	Proposed
Implementation	- PI controller using FOC technique - manual VHDL coding	- PI controller using FOC technique -Verilog HDL manual coding	- PI controller using FOC technique -Verilog HDL manual coding	- Model predictive Control with two time scale optimization -VHDL HDL manual coding	- PI controller using FOC technique -VHDL coding using HDL coder
Device	-FPGA Xilinx Spartan6	- FPGA Altera Stratix IV	- Altera Cyclone III FPGA	- FPGA ZYNQ 7000 processor	- Xilinx Virtex5 Xc5vlx50t
Area	-Slice Registers 1521/54576(2%) - Slice LUTs 6117/27288 (22%) - fully used LUT-FF pairs 1460/ 6178 (23%)	- Total logic elements 1182/182,400 (<1%) - combinational functions 1185/182,400 (<1%)	_______	- I/O cells 43/125(34.4%) - LUTs 6084/53200 (11.44%)	- I/O cells 148/480(30%) - Slice Registers 64/28,800 1% - Fully used LUT-FF pairs 64/1,177 (5%), - Occupied slice 364/7200 5%
Execution Time	_______	50ns	50us	0.7 us	20.875ns
Frequency	_______	40MHz	20 kHz	0.142.857 MHz	47.945 MHz

IX. CONCLUSION

A precise, cost effective, simple and high-speed implementation of Field oriented control of PMSM using the HDL Coder is presented in this work. Hardware generated code with HDL coder proves that the HDL Coder offers a very efficient platform in rapidly prototyping the model on a FPGA platform. The design methodology is easy, faster, and provides a great degree of confidence as compared to the hand coding which is error prone and takes long developing cycle. The implemented design on Virtex5 FPGA utilizes less available hardware resources and provides the possibility of implementation of some more parallel processes on the same FPGA device. The estimated 47.945MHZ frequency is obtained, which is more than enough for FOC controller of PMSM drive. Besides this, proposed design is validated with the existing works. Thus, this FPGA realization is a rapid solution and reveals that the overall motor system and performance of FOC PMSM has been improved in terms of its efficiency and stability.

REFERENCES

[1] W. Liu and P. Xu, “Design of PMSM Speed Control system based on Simulink Model,” IOP Conf. Ser. Material Science and. Engineering vol. 569, no. 4, 2019.

[2] Y. M. Alsayed, A. Maamoun and A. Shaltout, "High Performance Control of PMSM Drive System Implementation Based on DSP Real-Time Controller," in proceedings of 20*19 International Conference on Innovative Trends in Computer Engineering (ITCE)*, Aswan, Egypt, pp. 225-230, 2019.

[3] V. M. Bida, D. V Samokhvalov, and F. S. Al-mahturi, “PMSM Vector Control Techniques – a Survey,” in proceedings of 2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus), **Moscow**, Russia, pp. 577-581, 2018.

[4] T. Rudnicki, “Measurement of the PMSM current with a current transducer with DSP and FPGA,” Energies, vol. 13, no. 1, pp. 1–16, 2020.

[5] P. Ramesh and R. Prathyusha , “Field Oriented Control of Permanent Magnet Synchronous Motor,” International Journal of Computer Science and Mobile Computing (IJCSMC) , vol.3, no.3, pp. 269-275, 2014.

[6] B.Tufekci, B. Onal, H. Dere and H. F. Ugurdag, "Efficient FPGA Implementation of Field Oriented Control for 3-Phase Machine Drives," in proceedings of *2020 IEEE East-West Design & Test Symposium (EWDTS)*, Varna, Bulgaria, pp.1-5, 2020.

[7] A.Samat, P.Saedin, A. I.Tajudin, N.Adni P. Pauh, and P. Pinang “The Implementation of Field Oriented Control for PMSM Drive Based on TMS320F2808 DSP Controller”, in proceedings of IEEE International Conference on Control System, Computing and Engineering, Penang, Malaysia, pp.612-616, 2012.

[8] X. Zhang, X. Xie, and R. Yao, “Field Oriented Control for Permanent Magnet Synchronous Motor Based on DSP

Experimental Platform," in proceedings of 27th Chinese Control and Decision Conference (2015 CCDC), Qingdao, pp. 1870-1875, 2015.
[9] M.Skiwski, T.Tarczewski, L. M. Grzesiak, "PMSM Drive Based on STM32F4 Microcontroller", Poznan University of Technology Academic Journals, vol.87, pp. 377-387, 2016.
[10] X. Wang, M. Reitz, and E. E. Yaz, "Field Oriented Sliding Mode Control of Surface-Mounted Permanent Magnet AC Motors: Theory and Applications to Electrified Vehicles," IEEE Transactions on Vehicular Technology, vol. 67, no. 11, pp. 10343–10356, 2018.
[11] S. Gao and H. Zhao, "The research of permanent magnet synchronous motor drive based on the IGBT intelligent power module," in proceedings of 30th Chinese Control Decision Conference CCDC 2018, pp. 2879–2883, 2018.
[12] M. W. Naouar, A. A. Naassani, E. Monmasson, and I. Slama-Belkhodja, "FPGA-based predictive current controller for synchronous machine speed drive," IEEE Transactions on Power Electronics, vol. 23, no. 4, pp. 2115–2126, 2008.
[13] M. Marufuzzaman, M. B. I. Reaz, L. F. Rahman, and T. G. Chang, "High-speed current dq PI controller for vector controlled PMSM drive," Scientific World journal, vol. 2014.
[14] C. K. Lai, Y. T. Tsao, and C. C. Tsai, "Modeling, analysis, and realization of permanent magnet synchronous motor current vector control by MATLAB/simulink and FPGA," Machines, vol. 5, no. 4, 2017.

C. K. Lai, Y. T. Tsao, and C. C. Tsai, "

[15] F.Ramirez, M.Pacas, C Gonzalez, "FPGA-based Sensor less Control of a PMSM at Low-Speed Range", in proceedings of 2017 International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), Nuremberg, Germany, pp.121-128, 2017.
[16] V. P. Virani, S. Arya, and J. . Baria, "Modelling and Control of PMSM Drive by Field Oriented Control For HEV," SSRN Electronic Journal, pp.1–11, 2019.
[17] F. Amin, E. Bin Sulaiman, W. M. Utomo, H. A. Soomro, M. Jenal, and R. Kumar, "Modelling and simulation of field oriented control based permanent magnet synchronous motor drive system," Indonesian Journal of Electrical Engineering and Computer Science, vol.6, no.2, pp. 387 – 395, 2017.
[18] C. Ogbuka, C. Nwosu, and M. Agu, "A high performance hysteresis current control of a permanent magnet synchronous motor drive," Turkish Journal of Electrical Engineering & Computer Sciences, vol. 25, no. 1, pp. 1–14, 2017.
[19] F. MEMON, F. JAMEEL, M. ARIF, F. A. MEMON, "Model Based FPGA Design of Histogram Equalization", Sindh University research Journal (Science Series), vol. 48, no.2, pp. 435-440,2016
[20] Y. P. Siwakoti and G. E. Town, "Design of FPGA-controlled power electronics and drives using MATLAB Simulink," in proceedings of 5th IEEE Annual International Energy Conversion Congress and Exhibition (ECCE), Melbourne, VIC, Australia, pp. 571-577, 2013.
[21] W. Tu, G. Luo, Z. Chen, C. Liu, and L. Cui, "FPGA Implementation of Predictive Cascaded Speed and Current Control of PMSM Drives With Two-Time-Scale Optimization," IEEE Transactions on Industrial Informatics, vol. 15, no. 9, pp. 5276–5288, 2019.