

Performance Evaluation of Three Phase Five Level Inverter with Switched DC Sources

Bilal Ahmed¹

Department of Electrical Engineering Mehran University of Engineering and Technology Jamshoro Sindh, Pakistan

Corresponding author e-mail: (Bilal.ahmed.be13@iba-suk.edu.pk)

[Received on: 30-01-2021 Accepted on: 08-02-2021 Published on: 18-02-2021]

Abstract—Multilevel inverters have got very much popularity in last few decades. There are many topologies of inverter, keeping in view the efficiency and reduced circuit complexity. This paper mainly focuses on reduce device count of an inverter with switched DC sources proposed topology. This paper presents an analytical analysis of three phase five level switched DC sources inverter. The multicarrier pulse width modulation techniques like phase opposition, phase disposition and phase opposition disposition are compared with improved efficiency in MATLAB/SIMULINK. Switched DC source topology results in less number of switching devices as compared to classical topology. The topologies are compared according to their output voltage, output current, and total harmonic distortion (THD).

Index Terms— Switched DC sources, cascaded H-bridge, POD, total harmonic distortion, pulse width modulation (PWM).

I. INTRODUCTION

Inverters are fundamental devices to convert DC supply to AC source. There are many devices that cannot work properly without low-distorted sine wave supply. To cope-up with this problem, the sinusoidal pulse width modulation scheme is used to extract pure sine wave at the output. Input DC supply can be taken from many sources such as battery, photovoltaic array, magneto hydrodynamic generator, fuel cell, power supply network, or rectifier of rotating alternator etc. [1]. This constant supply is converted to variable width (pulse width modulation) with constant frequency. Later on, it is provided to power switches for proper shaping of sinusoidal signal. There are different types of modulation schemes like; saw tooth PWM, linear modulation, and sinusoidal pulse width modulation (SPWM) [2]. To get pure sine wave at the output, SPWM is widely used because of multiple advantages such as reduced filter size, less harmonics, cost effective, low distortion factor etc. [3-5]. Furthermore, the multilevel waveform has a better harmonic handling capability as compared to a two-level waveform obtained from conventional inverters. MLIs are advantageous due to reduced dv/dt affect on the user end load and high bearing capability of fault-tolerant operation [6-8]. The conventional inverters like, multilevel inverters which are mostly comprises of H-bridge cells connected in series to synthesize a required voltage from number of separate DC sources which may be attained from batteries or fuel cells. All these properties of cascaded inverters provide us a platform by using various pulse width modulation (PWM) schemes to control the working performance of an inverter efficiently [9-13]. Those pure sine wave inverters are used for

uninterruptable power supplies (UPS), AC motor drives, HVDC transmission lines, standby aircraft power supplies.

The arrangement of this paper is divided in various sections mentioned as. In Section II the MATLAB simulation of three phase five level inverter with switched DC sources are presented. The section III illustrates the three phase output voltage and its total harmonic distortion for each phase. In Section IV, description of a control scheme based on multicarrier pulsewidth modulation (PWM) is given. In last the Conclusions are concluded in Section V.

II. SIMULATION OF THREE PHASE FIVE LEVEL INVERTER WITH SWITCHED DC SOURCES INVERTER

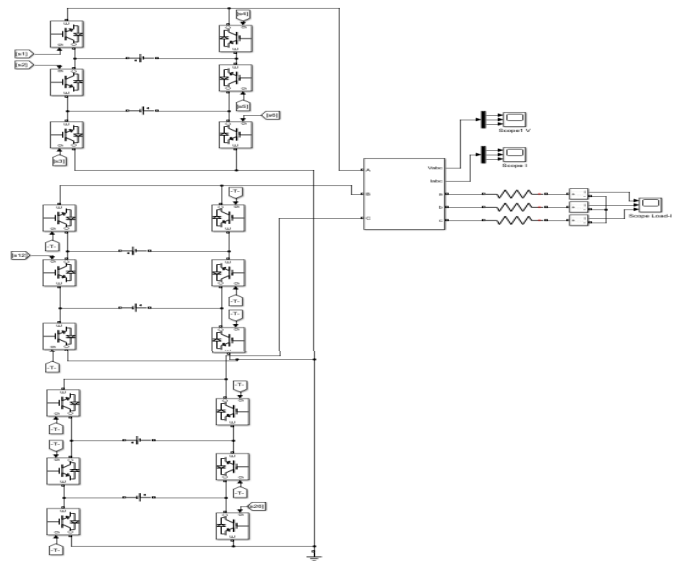


Fig. 1. MATLAB/SIMULINK Model of three phase inverter with Switched DC sources.

In this model IGBTs are used as switching devices with an antiparallel diode. Input DC voltages are used as symmetric DC voltage sources three phase inverter. The IGBTs (insulated gate bipolar transistor) are placed with complementary pairs as (T_j, T'_j). Each phase has three pairs of active switches, if T_1 is in on condition the T'_1 must be in off condition for proper switching operation of inverter. IGBTs are operated on multilevel carrier signals having switching frequency of 1 kHz. In this topology multiple isolated input DC sources are alternately connected in opposite polarities through IGBTs the power switching devices. These sources are added individually or in combined form to produce three phase five

level staircase output voltage. The Simulink model is designed for three phase five level inverter with switched DC sources. This approach downsizes the power switching devices as compared to classical topologies. As we increase the voltage sources the number of output levels will be increased $N=2n+1$ where n is number of DC sources and N is number of output levels. The input DC sources are denoted as E_j (where j from 0 to n) and current from the sources are denoted as $i_j(t)$. The voltage across IGBTs is considered as nodal voltage and the voltage across load will be considered as load voltage. By adopting this technology the number of switching devices are reduced for performing the same operation as compared with classical topologies. This topology is most suitable for battery powered applications.

III. THREE PHASE OUTPUT VOLTAGE AND TOTAL HARMONIC DISTORTION (THD)

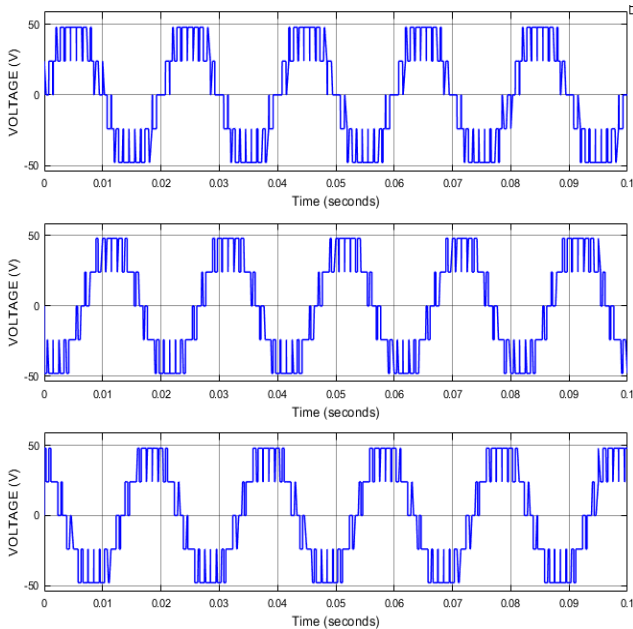


Fig. 2. Three Phase Output Voltage Waveform

In Fig.2, three phase five level output voltage waveform of switched DC sources is shown with POD carrier scheme. It can be clearly seen in Fig.2 that each phase voltage is having 120° phase shift from each other. The produced output voltage has symmetrical DC sources, $V_{out} = \pm 2V_{dc}$ for each phase. The output voltage of proposed topology is shown using phase opposition disposition carrier scheme. The five level output voltage wave form is generated on resistive load having switching frequency of 1 kHz and modulation of index as 1. The output voltage can be utilized for three phase load as well as for single phase load according to the requirement

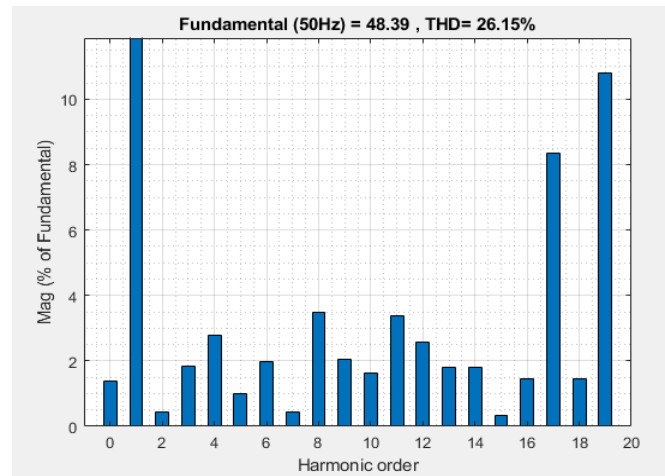


Fig. 3. Output Voltage THD For Phase-A

The total harmonic distortion for out voltage of phase-A is 26.15% which is shown in Fig.3. The harmonics are obtained at fundamental frequency of 50Hz and sampled at Nyquist frequency. At x-axis harmonic order is mentioned and on y-axis the magnitude of harmonic is mentioned.

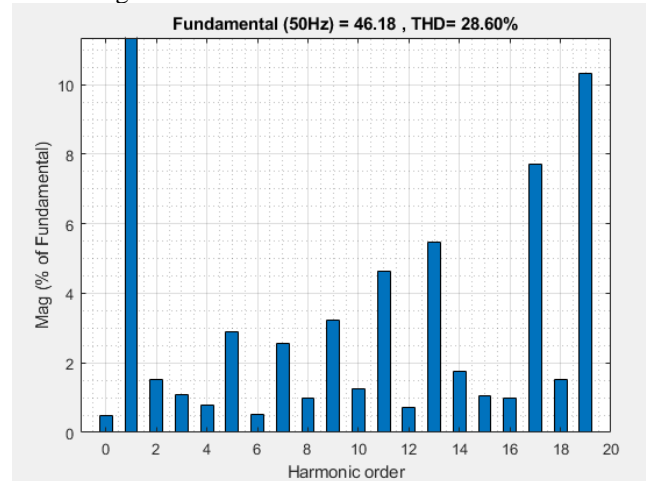


Fig. 4. Output Voltage THD For Phase-B

The total harmonic distortion of output voltage for phase-B is 28.60% which is shown in Fig. 4. The harmonics are obtained at fundamental frequency of 50Hz and sampled at Nyquist frequency. The significance of harmonics decreases as the order of harmonic increases. The magnitude of harmonics is mentioned at y-axis and harmonic order is mentioned x-axis.

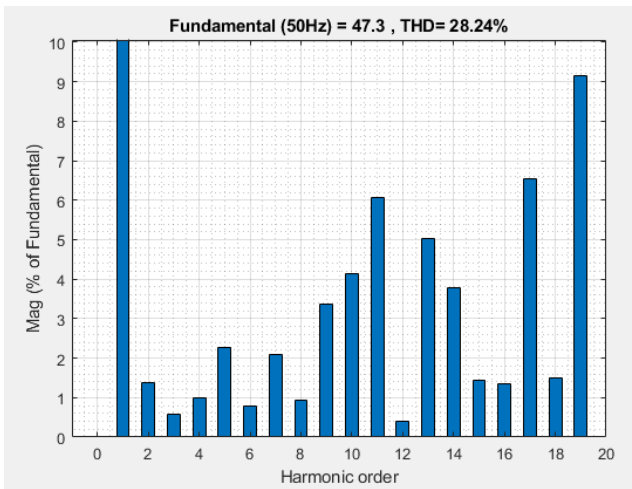


Fig. 5. Output Voltage THD For Phase-C

The Fig.5, gives the illustration about THD of five level output voltage for phase-C, which is 28.24%. The harmonics are produced at fundamental frequency of 50Hz. At x-axis harmonic order is mentioned and on y-axis the magnitude of harmonic is mentioned.

IV. CONTROL SCHEME BASED ON MULTICARRIER SINUSOIDAL PULSEWIDTH MODULATION (PWM)

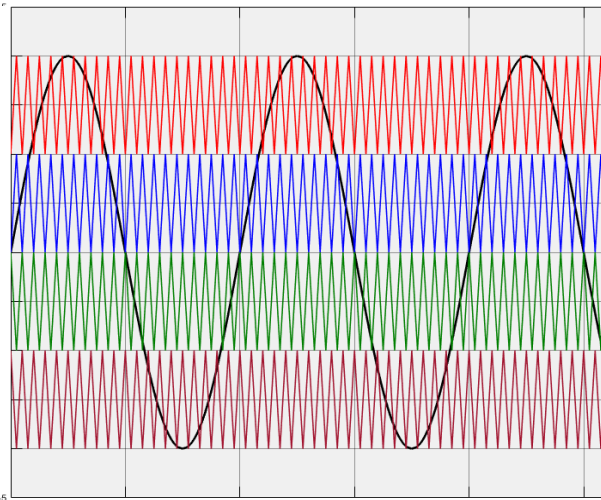


Fig. 6. Multicarrier Sinusoidal PWM scheme

Multicarrier sinusoidal PWM is most commonly used technique. Pulse width modulation techniques are adopted to perform the control operation of an inverter with respect to its voltage and current. In the above mentioned figure the phase opposition disposition scheme is given which is used for the switched DC source inverter. All the carrier signals which are above the zero reference value of sinusoidal point are at 180° out of phase with those which are below the zero reference point value. Sinusoidal signal is used as reference signal, upper two carrier waves are used for producing the positive peak of inverter which is $2V_{dc}$ and on contrary the lower two carrier signal are used for producing the negative peak of inverter which is $-2V_{dc}$ ($V_{dc}=12\text{volt}$). Here we have four carrier signals hence five levels are produced ($N=n+1$) where N is number of levels and n is number of carrier signal.

TABLE: I Component requirements and total voltage stress (N is number of levels in Phase voltage).

Inverter Type/Component	Cascaded H-bridge	Switched DC source
Number of main switches	$6(N-1)$	$3(N+1)$
Number of main diodes	$6(N-1)$	$3(N+1)$
Total component count	$27/2(N-1)$	$(15N+9)/2$

In this table it is clearly analyzed that the number of power switches requirement is less in case of switched DC source as compared to cascaded H-bridge. Therefore less power is dissipated through IGBTs. When devices are in conducting mode and switching mode, hence efficiency and reliability is increased.

V. CONCLUSION

Multilevel inverters are getting more interest in recent times, researchers are trying different topologies and scheme to increase output levels by reducing component counts. In this research paper the performance of three phase inverter in evaluated with the switched DC sources topology which is reduced component requirement topology. The performance is analyzed on the basis of inverter's three phase output voltage, their THD, and component count. Simulation results are performed on three phase five level inverter with proposed topology by using MATLAB. The analysis illustrates that the switched DC sources topology has certain advantages over conventional topologies therefore switched DC sources topology is highly competitive but it has two major limitations 1) the number of isolated DC sources required as in case of CHB and 2) lessens the bearing capability for fault-tolerant and reduced modularity as compared to CHB topology.

REFERENCES

- [1] Zope, Pankaj H., et al. "Design and Implementation of carrierbased Sinusoidal PWM Inverter," International Journal of advanced research in electrical, electronics and instrumentation engineering, vol. 1, no. 4, pp.230- 236, 2012.
- [2] Coppola, Marino, et al. "An FPGA-based advanced control strategy of a gridtied PV CHB inverter," IEEE Transactions on Power Electronics vol. 31, no. 1, pp. 806-816, 2016.
- [3] Mahar, Mukhtiar Ahmed, Muhammad Aslam Uqaili, and Abdul Sattar Larik. "Harmonic analysis of ac-dc topologies and their impacts on power systems." Mehran University Research Journal of Engineering & Technology vol. 30, no. 1 pp. 173-178, 2011.
- [4] Mahar, M.A, Larik, A.S and Shah, A.A. "Impacts on power factor of ac voltage controllers under nonsinusoidal conditions." Mehran University Research Journal of Engineering and Technology, vol. 31, no.2, pp. 297-300.
- [5] Maheshri, Sachin, and Prabodh Khampariya. "Simulation of single phase SPWM (Unipolar) inverter," International Journal of Innovative Research in Advanced Engineering (IJIRAE) vol. 1, no. 3, 2014.
- [6] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 906–918, Mar. 2013.

- [7] *Gupta, Krishna Kumar*, et al. "Multilevel inverter topologies with reduced device count: A review." *IEEE Transactions on Power Electronics* vol. 31, no. 1, pp. 135-151, 2016.
- [8] *J. Rodriguez, J.-S. Lai, and F. ZhengPeng*, "Multilevel inverters: A survey of topologies, controls, applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [9] *J. Ebrahimi, E. Babaei, and G. B. Gharehpetian*, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655–667, Feb. 2012.
- [10] *Prasad, G. Ranjith kumar, T.Vamsee kiran, G. Satya Narayana* "Comparison of different topologies of cascaded h-bridge multilevel inverter k.n.v". International Conference on Computer Communication and Informatics (ICCCI -2013), Jan. pp. 1–6, 2013.
- [11] *Ahmed, Mahrous, Ahmed Sheir, and Mohamed Orabi*. "Asymmetric cascaded half- bridge multilevel inverter without polarity changer." *Alexandria engineering journal*, vol. 57, no. 4, pp. 2415-2426, 2017.
- [12] *Fri A, El Bachtiri R, El Ghzizal A*. "A comparative study of three topologies of three-phase (5L) inverter for a PV system,". *Energy Procedia*, vol. 1, no. 42, pp. 436-445, 2013.
- [13] *Gupta, K.K. and S. Jain*, "A novel multilevel inverter based on switched DC sources". *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7 pp. 3269-3278, 2014.
- [14] *Dewangan, N.K., Gupta, S. and Gupta, K.K.*, "Fault-tolerant operation of some reduced-device-count multilevel inverters with improved performance". *International Transactions on Electrical Energy Systems*, vol. 29, no. 2, pp. 2731, 2019.
- [15] *Colak, I., E. Kabalci, and R. Bayindir*, "Review of multilevel voltage source inverter topologies and control schemes". *Energy conversion and management*, vol. 52, no. 2, pp. 1114-1128, 2011.
- [16] *E. Najafi and A. H. M. Yatim*, "Design and implementation of a new multilevel inverter topology," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, Nov. 2012.
- [17] *P.V Kumar, C.S Kumar and K.R Reddy* "Single Phase Cascaded Multilevel Inverter using Multicarrier PWM Technique", *ARNP Journal of Engineering and Applied Sciences*, vol. 8, no. 10, 2013.
- [18] *Solangi, Muzamil Hussain, Mukhtiar Ahmed Mahar, Abdul Sattar Larik, and Mohsin Raza Mahessar*. "Design a Perturb & Observe MPPT Algorithm for PV System Based Asymmetric Cascaded Half-Bridge Multilevel Inverter." *INDIAN JOURNAL OF SCIENCE AND TECHNOLOGY* vol. 13, no. 04, pp. 439-452, 2020.